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A Novel Five-Level Voltage Source Inverter with Sinusoidal Pulse Width Modulator for Medium-Voltage Applications

Mehdi Narimani, *Senior Member, IEEE,* Bin Wu, *Fellow Member,* Navid Reza Zargari, *Fellow Member, IEEE*

***Abstract*— This paper proposes a new five-level voltage source inverter (VSI) for medium-voltage high-power applications. The proposed inverter is based on the upgrade of a four-level nested neutral-point clamped (NNPC) converter. This inverter can operate over a wide range of voltages without the need for connecting power semiconductor in series, has high quality output voltage and fewer components compared to other classic five-level topologies. The features and operation of the proposed converter are studied and a simple sinusoidal PWM scheme is developed to control and balance the flying capacitors to their desired values. The performance of the proposed converter is evaluated by simulation and experimental results.**

***Index Terms*— Multilevel converter, DC–AC power conversion, sinusoidal pulse width modulation (SPWM).**

I. Introduction

For high-power medium-voltage (MV) industrial applications, multilevel converters are the best candidates and this is because multilevel topologies can synthesize near sinusoidal voltage with low harmonic distortion that reduces the size of output filter. These topologies have also low switch stress, reduced common mode voltage, and high voltage capability [1]-[4].

The diode clamped converter (DCC), flying capacitor converter (FC), and the cascaded H-bridge (CHB) converter are the most well-known multilevel converter topologies [2] that have been commercialized successfully by major manufacturers. However, these topologies have some drawbacks which limit their applications for more levels. DCC topology with more number of levels is less attractive because of its limitations; 1) dc-link capacitor voltage balance becomes unattainable in higher level topologies with a passive front end, and 2) the number of clamping diodes increases substantially with the voltage level [5]. Flying Capacitor (FC) topology needs to have higher switching frequencies to keep the capacitors properly balanced, whether a self-balancing or a control-assisted balancing modulation method is used. Also the number of flying capacitors increases with the voltage level. Although cascade H-Bridge (CHB) topology can reach higher voltage and higher power levels with modular structure, this topology needs a number of isolated dc sources, an expensive and bulky phase-shifting transformer, and a substantially more number of active devices to achieve a regenerative operation.

A number of new multilevel converters for more levels have been proposed in literature [6]-[22]. These are variations or hybrids of the three major multilevel topologies. Among the existing topologies, the following topologies with five-level structure have found practical applications which are commercialized by manufacturers; the five-level H-bridge NPC (5L-HNPC) and the five-level active NPC (5L-ANPC). The main features of these converters are:

- A five-level H-bridge NPC (5L-HNPC) is the H-bridge connection of two classic 3L-NPC phase legs [6]-[8]. This topology requires three isolated dc sources fed by a phase shifting transformer and a number of diode bridges. The bulky phase shifting transformer increases also cost and complexity of the converter.
- A five-level active NPC (5L-ANPC) is a combination of a 3L-ANPC and 3L-FC, which increases the number of voltage levels [9]-[13]. This converter can reach more output levels. The main drawback of the 5L-ANPC is that the voltage rating of the power semiconductors are different; the outer switches are subjected to half of the dc-link voltage but the inner devices have only one fourth of the dc-link voltage. This limits the voltage rate of the converter for higher voltage applications.
- A five-level diode-clamped converter [5], [14]-[17] which has a large number of clamping diodes. This converter has 36 diodes, 12 diodes in each phase. Voltage balancing of the dc-link capacitors is another issue with this topology which has been studied comprehensively in [5].
- A five-level Flying Capacitor (FC) converter [18]-[20]. In this converter there are two main issues; the number of flying capacitor and regulating voltages of the flying capacitors. In practical applications, the manufacturers try to reduce the number of capacitors.

Recently, a novel four-level nested neutral point clamped (NNPC) converter has been proposed in [21]. This topology has interesting properties such as operating over a wide range of voltages (2.4-7.2kV) without the need for connecting power semiconductor in series, all switches have the same voltage stress (equal to one third of the dc voltage), and fewer components compared to other classical four-level topologies. However, this topology is a four-level topology.

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In this paper, a new five-level voltage source converter that is based on the upgrade of a four-level NNPC converter is proposed. This inverter, compared to other classic five-level topologies, can operate over a wider range of voltages without the need for connecting power semiconductor in series and it also has fewer components. The proposed five-level converter mitigates the drawbacks of the previous five-level converters. This converter has the following features;

1. The number of clamping diode has been reduced significantly compared to five-level DCC converter. A five-level DCC converter has 12 diodes in each phase however the proposed topology needs 2 diodes per phase [5].
2. It has fewer flying capacitors compared to five-level FC converter.
3. Unlike 5L-HNPC converter, the proposed converter does not need any isolated DC source that makes the converter appropriate for regenerative applications.
4. Unlike 5L-ANPC, the voltage stresses of the power switches are the same and they are equal to quarter of the input dc-link voltage.

The proposed five-level converter is studied and analyzed in this paper. A novel and simple SPWM techniques is also developed for the proposed converter to control and balance the capacitor voltages. The performance of the converter under different operating conditions is investigated in MATLAB/Simulink environment. The feasibility of the proposed converter is verified by a scale-down prototype converter.

II. Converter Topology

A. Operation of the Proposed Five-Level Voltage Source Invrerter

The proposed multilevel topology, as shown in Fig. 1, is based on the upgrade of a four-level nested neutral-point clamped (NNPC) converter. To ensure equally spaced steps in the output voltages, the capacitor Cx_1 and Cx_2, $x=a,b,c$ are charged to $1/4V_{dc}$ and C_{x3} is charged to $3/4V_{dc}$.

Five output levels are achieved from twelve distinct switching combinations. The list of switching combinations is shown in Table I. It should be noted that the voltage stresses across the switches do not exceed 1/4 of dc-link voltage. Another advantage of the proposed converter is the redundancy in switch combination to generate the output levels. For example, there are three redundant switching states (as can be seen from Table I) to generate voltage levels of $1/4V_{dc}$ and $-1/4V_{dc}$ and there are four redundant switching states to generate voltage levels of zero (0). Each redundant state provides a charging and discharging current path for each floating capacitor. This feature of redundant switching states can be used to achieve voltage balancing of the capacitors.

B. SPWM Scheme for the Proposed Five-Level Inverter

One of the most popular modulation scheme in industry applications is Sinusoidal PWM (SPWM). This modulation scheme is based on multicarrier PWM strategy. In this section, a new approach is proposed to use the multicarrier SPWM strategy to generate multilevel output voltage while regulating the voltage of flying capacitors. This approach employs the

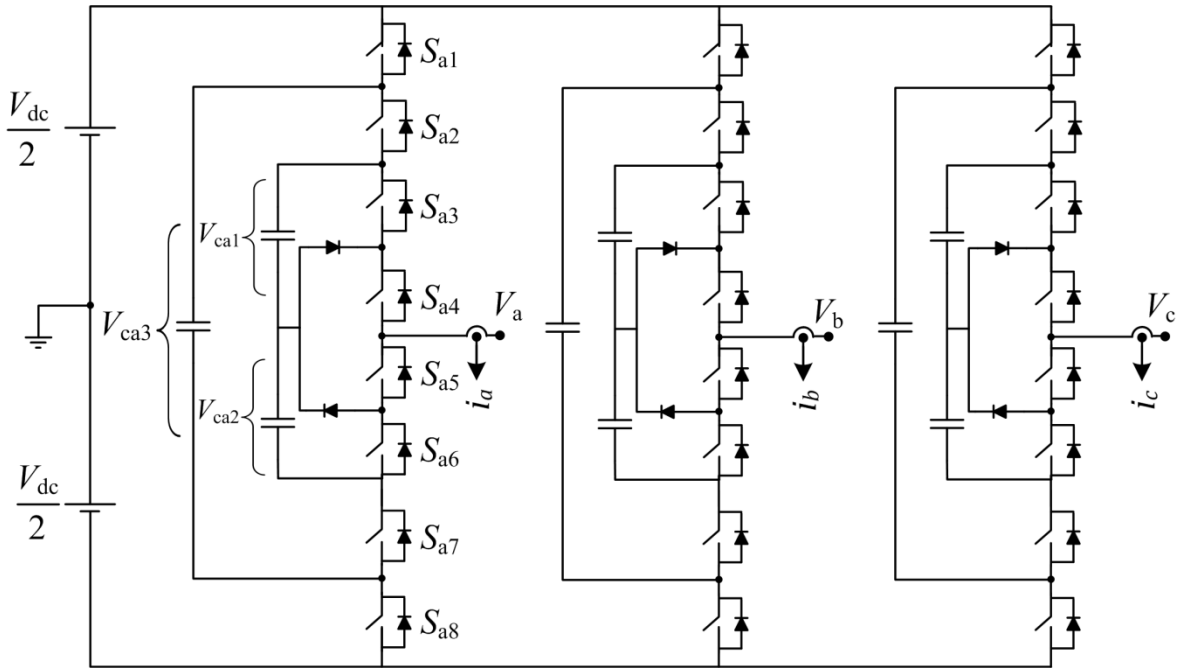

Fig. 1. A new five-level three-phase inverter.

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TABLE I: SWITCHING STATES OF THE PROPOSED FIVE-LEVEL CONVERTER AND CONTRIBUTION OF THE AC-SIDE CURRENTS TO THE FLYING CAPACITOR VOLTAGES

State	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{Cx1}		V_{Cx2}		V_{Cx3}		V_{ax}	Level
									$i_x>0$	$i_x<0$	$i_x>0$	$i_x<0$	$i_x>0$	$i_x<0$		
E	1	1	1	1	0	0	0	0	-	-	-	-	-	-	$V_{dc}/2$	4
D3	1	1	0	1	1	0	0	0	C	D	-	-	-	-	$V_{dc}/4$	3
D2	0	1	1	1	0	0	0	1	-	-	-	-	D	C		
D1	1	0	1	1	0	0	1	0	D	C	D	C	C	D		
C4	1	1	0	0	1	1	0	0	C	D	C	D	-	-	0	2
C3	1	0	0	1	1	0	1	0	-	-	D	C	C	D		
C2	0	1	0	1	1	0	0	1	C	D	-	-	D	C		
C1	0	0	1	1	0	0	1	1	D	C	D	C	-	-		
B3	0	0	0	1	1	0	1	1	-	-	D	C	-	-	$-V_{dc}/4$	1
B2	1	0	0	0	1	1	1	0	-	-	-	-	C	D		
B1	0	1	0	0	1	1	0	1	C	D	C	D	D	C		
A	0	0	0	0	1	1	1	1	-	-	-	-	-	-	$-V_{dc}/2$	0

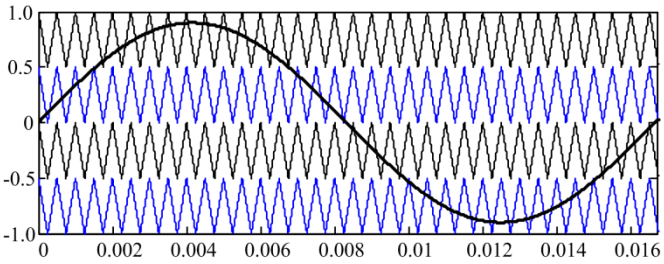
C: Charging D: Discharging

deviation of the capacitor voltages from their nominal values and based on the converter output current select the best switching state from the available redundant switching states to charge or discharge the capacitors and finally regulate the voltages of capacitors. This approach is intuitive and simple to implement in a digital control system.

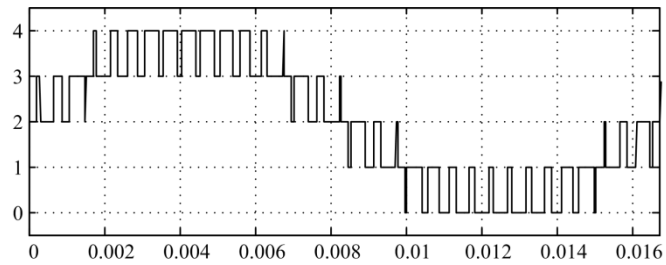
In this strategy, four level-shifted triangular carriers with in-phase disposition (IPD) method are employed, where all carriers are in phase and have the same magnitude as shown in Fig.2(a). Fig. 2(b) shows the desired output levels which is the result of comparing carriers and modulation signal. Based on the desired level at the output, the corresponding switching state can be selected from Table I and then applied to the power switches.

Table I also shows that there are redundancy states for level 1, 2 and 3. As can be seen from Table I, each redundancy state based on the direction of the output current can charge or discharge the flying capacitors and thus minimize the difference between the nominal voltage values and the measured voltage values. For example, when the desired output level is 3 and the capacitor C_{x3} needs to be charged, if the output current is positive the switching state D_1 should be chosen to charge the capacitor C_{x3} and if the output current is negative the switching state D_2 should be chosen.

If there is no control over the currents that flow into/out from the flying capacitors to charge/discharge the capacitors, therefore the voltage of the flying capacitors may deviate from their desired values.



(a) Level-shifted multicarrier modulation for a 5L FC-NNPC topology



(b) Desired output levels

Fig.2. Level-shifted multicarrier strategy for a five-level inverter

The voltage deviation of the flying capacitors can be expressed as:

$$\Delta V_{cxi} = V_{cxi} - V_{cxi,\,ref}\ ,\quad x = a, b, c, \text{ and } i = 1, 2, 3 \qquad (1)$$

where V_{Cxi} are the capacitor voltages, $V_{cxi,\,ref}$ are the nominal values which $V_{cxi,\,ref} = V_{dc}/4$ for i =1,2 and $V_{cx3,\,ref} = 3V_{dc}/4$. To achieve capacitor voltage balancing, the deviation ΔV_{Cxi} should be close to zero.

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As can be seen from the Table I, there are enough redundancy at level 1, 2 and 3 to charge and discharge the flying capacitors. Level 1 is a good candidate to control voltages of capacitor C_{x3} and C_{x2} while Level 3 is a good candidate to control voltage of capacitors C_{x3} and C_{x1}. Table II shows that which switching state should be chosen in different conditions to control voltage of flying capacitors. For example, if the level is 2 and the deviation of capacitor C_{x1} is more than other capacitors (($|\Delta V_{CX1}| > |\Delta V_{CX3}|$) & ($|\Delta V_{CX1}| > |\Delta V_{CX2}|$)), it means that the main priority should be given to charge or discharge capacitor C_{x1}. Assume that $i_x > 0$, if $\Delta V_{cx1} > 0$, therefore the capacitor C_{x1} should be discharged and thus the State C1 should be selected.

According to Table I and II, the procedure bellow should be followed to control the flying capacitor voltages:

1- The desired output level should be determined by comparing carriers and modulation signal, as shown in Fig. 2,

2- The direction of the phase current and voltages of the flying capacitors should be measured and then the capacitor voltage deviation can be determined based on (1),

3- and finally the appropriate switching state can be selected from Table II and the corresponding gating signals will be applied to the power semiconductors.

The flowchart shown in Fig.3 illustrates the procedure to control voltage of flying capacitors in each phase. First, the modulating signal for phase x (x=a,b,c) is compared to carriers (four carriers) and then the desired output levels are determined. If the desired output level (L) is 0 or 4, the corresponding switching state will be State A or E from Table I respectively. Otherwise, the capacitor voltages (V_{CX1}, V_{CX2} and V_{CX3}) and phase current (i_X) should be measured and then based on the output level (L) the appropriate switching state should be selected from Table II.

This procedure can be applied to each leg separately to control its flying capacitor voltages, the only difference is that modulating signals should have ±120° phase shift respect to each other. As can be seen, this procedure is very simple to implement in a digital controller.

TABLE II: THE PROPOSED VOLTAGE BALANCING METHOD FOR EACH PHASE OF THE FIVE-LEVEL INVERTER

Output Level	Condition	i_x	ΔV_{CX1}	ΔV_{CX2}	ΔV_{CX3}	State
3	$\|\Delta V_{CX1}\| > \|\Delta V_{CX3}\|$	≥ 0	≥ 0	-	-	D1
			< 0	-	-	D3
		< 0	≥ 0	-	-	D3
			< 0	-	-	D1
	$\|\Delta V_{CX3}\| > \|\Delta V_{CX1}\|$	≥ 0	-	-	≥ 0	D2
			-	-	< 0	D1
		< 0	-	-	≥ 0	D1
			-	-	< 0	D2
2	$\|\Delta V_{CX1}\| > \|\Delta V_{CX3}\|$ & $\|\Delta V_{CX1}\| > \|\Delta V_{CX2}\|$	≥ 0	≥ 0	-	-	C1
			< 0	-	-	C2 / C4
		< 0	≥ 0	-	-	C2 / C4
			< 0	-	-	C1
	$\|\Delta V_{CX2}\| > \|\Delta V_{CX1}\|$ & $\|\Delta V_{CX2}\| > \|\Delta V_{CX3}\|$	≥ 0	-	≥ 0	-	C3 / C1
			-	< 0	-	C2
		< 0	-	≥ 0	-	C2
			-	< 0	-	C3 / C1
	$\|\Delta V_{CX3}\| > \|\Delta V_{CX1}\|$ & $\|\Delta V_{CX3}\| > \|\Delta V_{CX2}\|$	≥ 0	-	-	≥ 0	C2
			-	-	< 0	C3
		< 0	-	-	≥ 0	C3
			-	-	< 0	C2
1	$\|\Delta V_{CX2}\| > \|\Delta V_{CX3}\|$	≥ 0	-	≥ 0	-	B3
			-	< 0	-	B1
		< 0	-	≥ 0	-	B1
			-	< 0	-	B3
	$\|\Delta V_{CX3}\| > \|\Delta V_{CX2}\|$	≥ 0	-	-	≥ 0	B1
			-	-	< 0	B2
		< 0	-	-	≥ 0	B2
			-	-	< 0	B1

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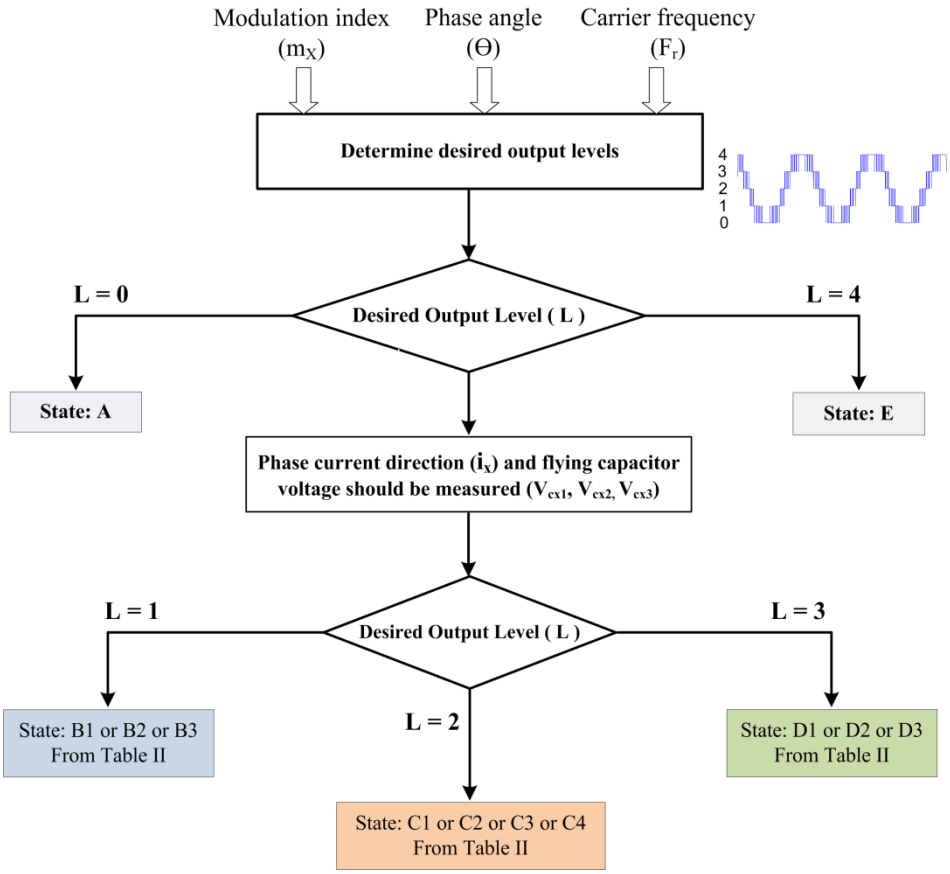

Fig.3. The procedure to control of flying capacitor voltages.

III. Simulation Results

In order to show the performance of the proposed five-level converter, simulation studies have be done in MATLAB/Simulink environment for a 5MVA/7.2kV inverter. The parameters of the system are shown in Table III. The simulation also demonstrates the effectiveness of the developed SPWM to generate output voltages and to regulate and balance the voltage of flying capacitors.

The performance of the proposed five-level converter and SPWM controller has been studied during both steady-state and transient-state conditions.

TABLE III: Parameters of the Study System (Simulation)

Converter Parameters	Values	Values (p.u)
Converter Rating	5 MVA	1.0
Output Voltage	7.2 kV	1.0
Flying Capacitors	1000 µF	4.0
Input DC Voltage	12 kV	-
Output Frequency	60 Hz	1.0
Output Inductance	5.0mH	0.1
Device Switching Frequency	500 Hz	

A. *Steady-State Analysis*

Figs. 4 and 5 show the performance of the proposed converter using developed SPWM technique with different modulation indexes. Fig. 4 shows the inverter output voltage, output currents and flying capacitor voltages where modulation index m = 0.95 and Fig. 5 also shows the inverter output voltage, output currents and flying capacitor voltages where modulation index m = 0.65. From Fig. 4, the output line-to-line voltage is 9-level and the capacitors are well balanced even with a low device switching frequency that is 500 Hz.

Figs. 6 and 7 show the performance of the proposed converter where the load is inductive with PF=0.7 and capacitive with PF=-0.7 respectively.

As can be seen from the Figs. 4 to 7, the proposed converter using SPWM can regulate and balance capacitor voltages under different conditions. It should be noted that the voltage stress for all the power switches are the same and equal to one-fourth of the dc-link voltage which in this case is 3000V.

B. *Transient-State Analysis*

In this case, step change from half-load to full-load at t = 0.15 sec has been applied to the power converter where m=0.95. As observed from Fig. 8, voltages of flying capacitors

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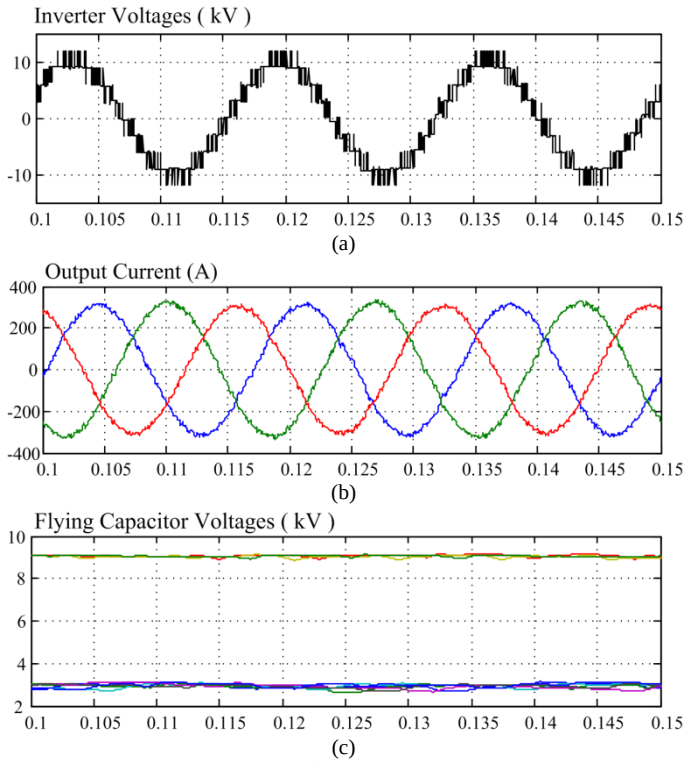

Fig. 4. Simulation waveforms in steady-state condition
(a) inverter voltage, (b) output currents, and (c) voltages of flying capacitors
(m=0.95)

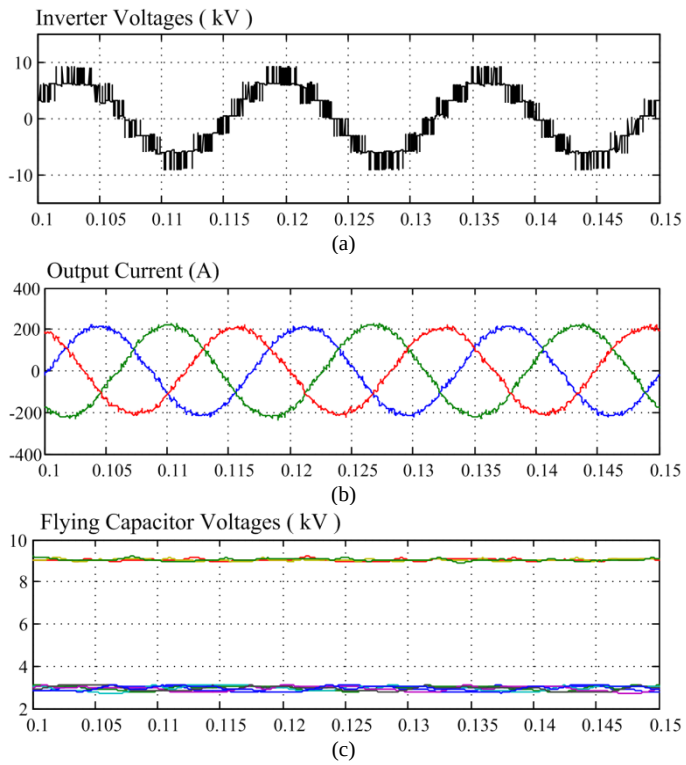

Fig. 5. Simulation waveforms in steady-state condition
(a) inverter voltage, (b) output currents, and (c) voltages of flying capacitors
(m=0.65)

are maintained at their nominal values. The nominal value for C_{x1} and C_{x2} is $1/4V_{dc}$ and that is $3/4V_{dc}$ for C_{x3}.

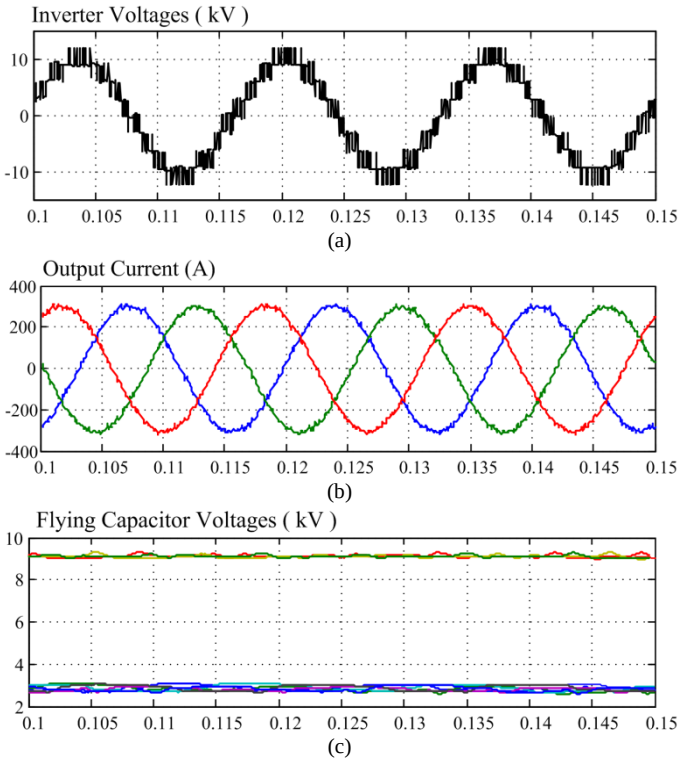

Fig. 6. Simulation waveforms in steady-state condition (inductive load)
(a)inverter voltage, (b)output currents, and (c)voltages of flying capacitors
(m=0.95, PF=0.7)

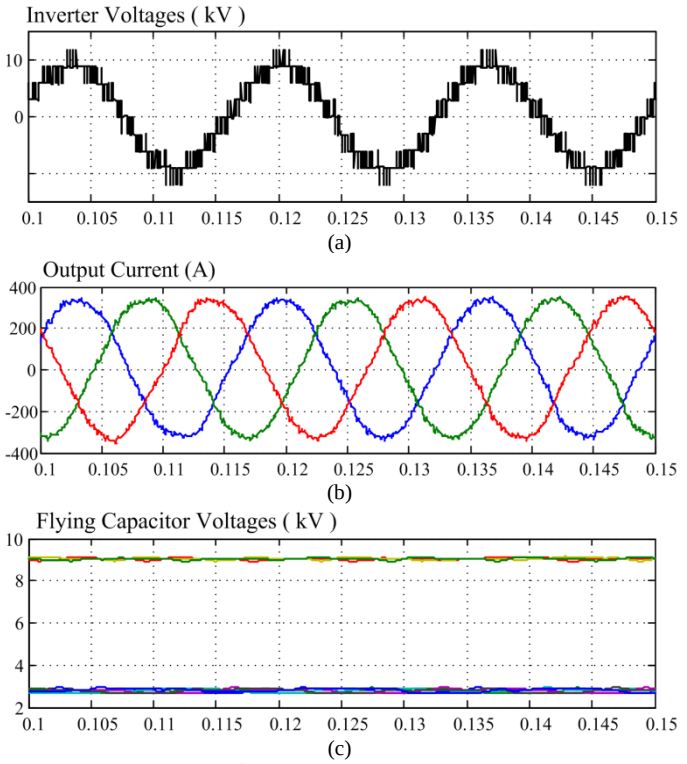

Fig. 7. Simulation waveforms in steady-state condition (capacitive load)
(a)inverter voltage, (b)output currents, and (c)voltages of flying capacitors
(m=0.9, PF=-0.7)

C. *Evaluation of Control Performance*

To show the performance of the controller, assume that the proposed converter is operating in normal condition and

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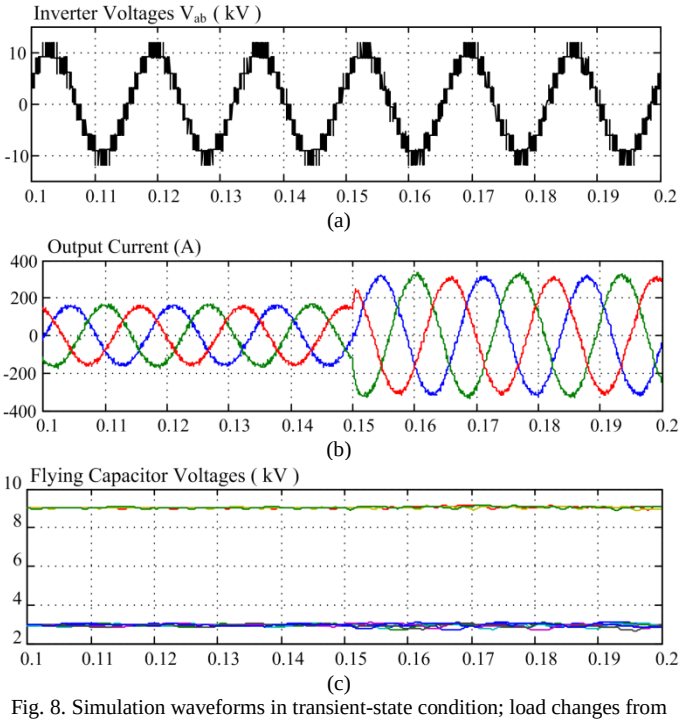

Fig. 8. Simulation waveforms in transient-state condition; load changes from half-load to full-load (a) inverter voltage, (b) output currents, and (c) voltages of flying capacitors (m=0.95)

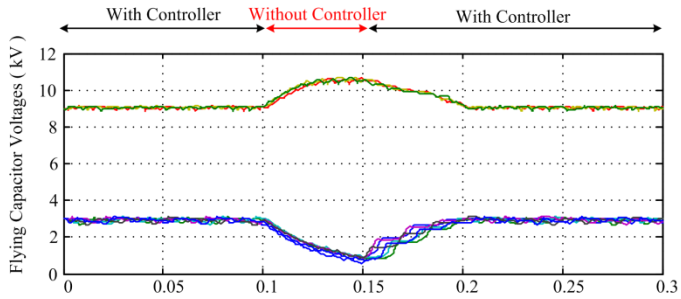

Fig. 9. Simulation waveforms; voltage of flying capacitors with and without the controller.

TABLE IV: PARAMETERS OF THE STUDY SYSTEM (EXPERIMENT)

Converter Parameters	Values
Converter Rating	5 kVA
Flying Capacitors	1000 µF
Input DC Voltage	300 V
Output Frequency	60 Hz
Output Inductor	5 mH
Device Switching Frequency	500 Hz

suddenly at t=0.1sec, the SPWM controller has been deactivated and at t=0.15sec the controller reactivated again.

As can be seen from Fig. 9, when the controller is deactivated the voltage of the capacitors deviate from the nominal values and when the controller reactivates the capacitor voltages start converging to their nominal values. This study shows the performance of the controller given by Table II.

IV. EXPERIMENTAL RESULTS

The feasibility of the proposed converter is evaluated experimentally. Fig. 10 shows the experimental setup for the proposed five-level inverter. The parameters of Table IV were used for experiments as a scaled-down prototype.

The converter switches, clamping diodes and gate drivers are developed by Semikron SKM75GB123D, SKKD75F12, and SKHI22B, respectively. The SPWM technique has been implemented by a dSPACE DS1103 rapid prototyping board and the gating signals are sent to the converters through an interface board consisting of MC14504BCP and TLP521-4.

The load currents and flying capacitor voltages were measured by LEM LA 100-P and LV 25-P transducers,

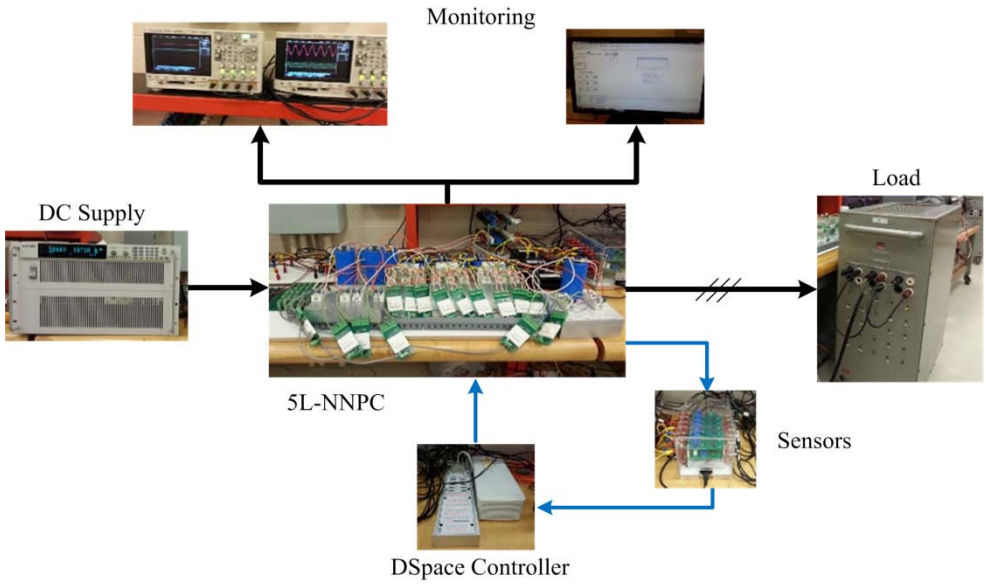

Fig. 10. Experimental setup for the proposed five-level inverter.

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respectively. To eliminate the effect of noise, digital low pass filters (<500Hz) are considered to eliminate the higher frequencies.

Figs. 11 and 12 show the performance of the proposed converter under different operating conditions. Fig. 11 shows the inverter output voltage, output currents and flying capacitor voltages where modulation index m = 0.95. Fig. 12 also shows the inverter output voltage, output currents and flying capacitor voltages where modulation index m = 0.65.

Fig. 13 shows the performance of the proposed converter under transient condition when load changes from half-load to full-load and Fig. 14 shows the effectiveness of the SPWM controller to control voltages of the flying capacitors. As can be seen from Fig. 11 to 14, in all cases capacitor voltages are well balanced and the feasibility of the five-level inverter is verified.

V. Conclusion

This paper introduces a new five-level voltage source inverter for medium-voltage applications. The proposed topology is the upgrade of the four-level NNPC converter that can operate over a wide range of input voltage without any power semiconductor in series. The proposed converter has

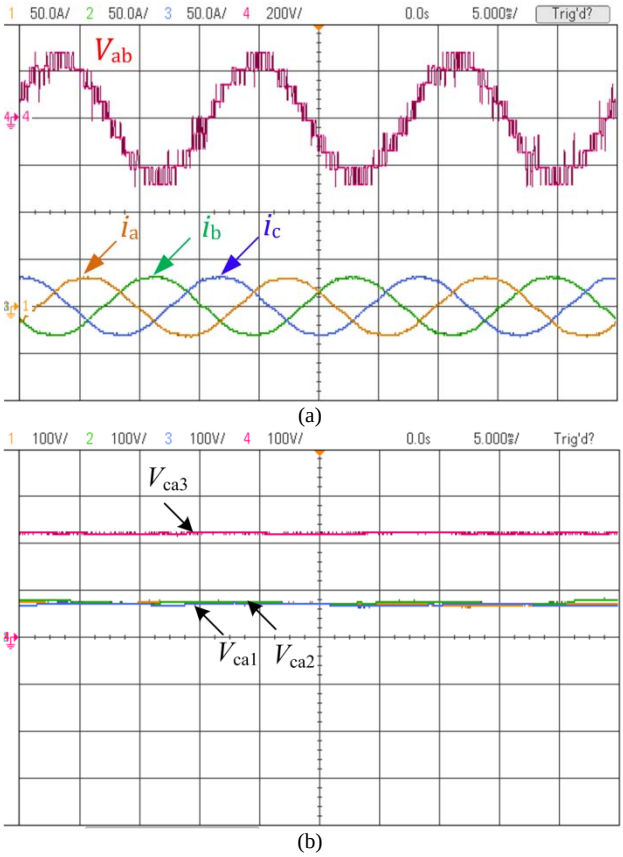

Fig. 11. Experimental results, steady state (a) inverter output line voltage and output currents (b) voltages of flying capacitors, m=0.95.

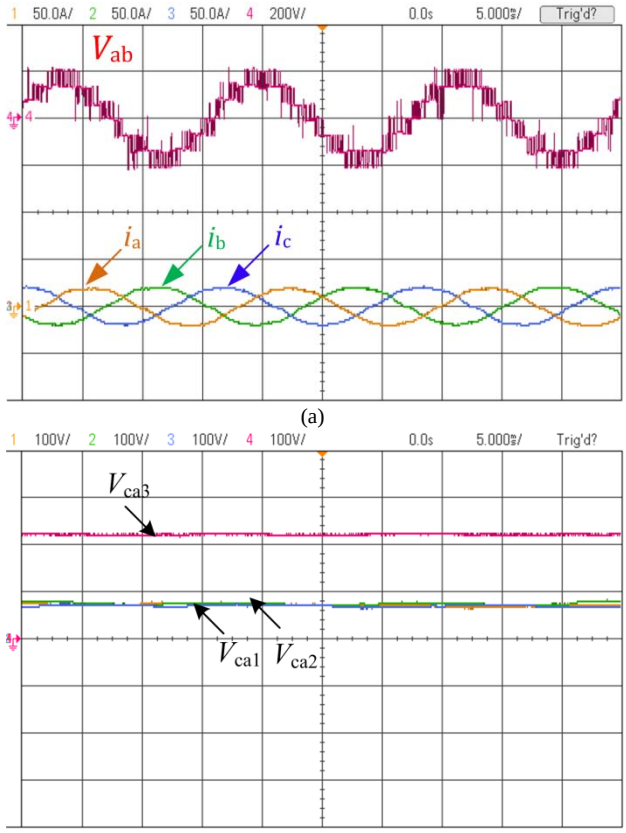

Fig. 12. Experimental results, steady state (a) inverter output line voltage and output currents (b) voltages of flying capacitors , m=0.65.

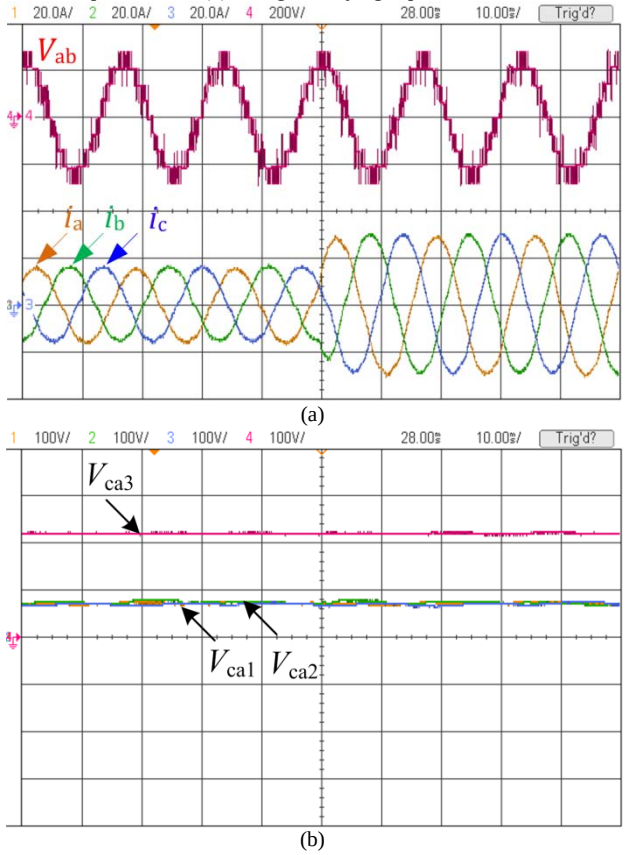

Fig. 13. Experimental results, transient state, (a) inverter output line voltage and output currents (b) voltages of flying capacitors, step change from half-load to full-load, m=0.95

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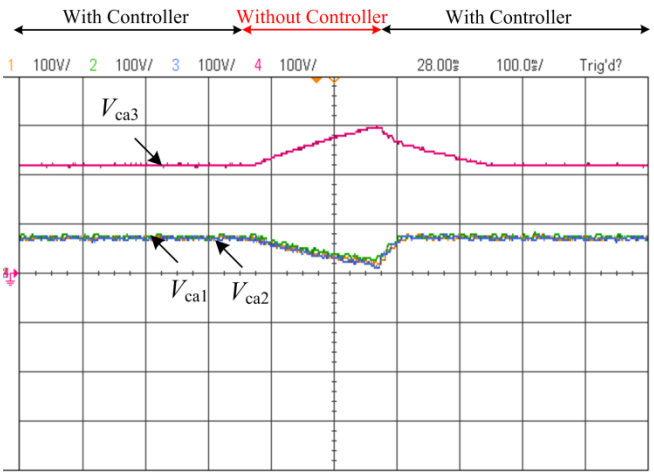

Fig. 14. Experimental results, the effectiveness of the SPWM controller to control voltages of flying capacitors.

fewer components as compared with classic multilevel converters and the voltage across the power semiconductors is only one-fourth of the dc-link. A SPWM strategy is developed to control the output voltage and regulate the voltage of the flying capacitors.

The proposed strategy is very intuitive and simple to implement in a digital system. The performance of the proposed converter is confirmed by simulation in MATLAB/Simulink environment and the feasibility of the proposed converter is evaluated experimentally and results are presented.

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